REMARKS

Claims 1-30 are pending in the present application, were examined, and were rejected. No claims are amended, added or cancelled. Applicant respectfully requests reconsideration of pending Claims 1-30 and in view of at least the following remarks.

I. Claims Rejected Under 35 U.S.C. §102

The Patent Office rejects Claims 1, 2, 10, 16, 22 and 26 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,742,788 to Priem et al. ("Priem1"). Applicant respectfully traverses this rejection.

Applicant respectfully asserts that the Examiner has failed to adequately set forth a *prima facie* rejection under 35 U.S.C. §102(b). "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik v. American Hoist & Derrick* ("Lindemann"), *730 F.2d 452, 1458 (Fed. Cir. 1994)*(emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. *Titanium Metals Corp. of American v. Banner* ("Banner Titanium"), *778 F.2d 775, 777 (Fed. Cir. 1985).*

Applicant submits that independent Claim 1 includes the following feature, which is neither taught nor suggested by either Priem1 or the references of record:

> a first frame buffer;
>
> a second frame buffer to store data used to refresh the display monitor. (Emphasis added.)

In contrast, and as clearly illustrated by careful review of FIG. 3, Priem1 provides:

> a single array of contiguous memory 42, which may be configured in various buffer arrangements in response to the software being run. The array 42, which may be configured into buffers, is constructed of VRAM and has two separate serial output terminals when providing data from a first portion (preferably half) of the array 42 and the other providing data from a second portion of the array 42 (col. 7, lines 51-57). (Emphasis added.)

Applicant submits that Priem1 teaches the use of a *single buffer with dual output ports* in contrast to first and second frame buffers, as required by Claim 1 of the invention.

Furthermore, Applicant submits that independent Claim 1 includes the following feature, which is neither nor suggested by either Priem1 or the references of record:

> a controller to copy identified data updated within the first frame buffer to the second frame buffer and a display monitor when the identified data is needed to refresh the display monitor. (Emphasis added.)

In contrast to the system described by Priem1, the controller copies identified, updated data within the first frame buffer to both the second frame buffer and the display monitor when the identified data is needed to refresh the display monitor as required by Claim 1.

In other words, data refresh is generally performed using the bandwidth of the second frame buffer. However, if data is updated within the first frame buffer, following completion of a most recent refresh cycle, such data is scanned or updated to the display monitor from the first frame buffer during a refresh cycle. As a result, refresh of updated data from the first frame buffer is concurrently performed.

In contrast, Priem1 requires:

> an invisible frame buffer of the array from which data is never scanned to the display 48 in the manner described in co-pending patent applications first mentioned above (col. 11, lines 5-9). (Emphasis added.)

Furthermore, Priem1 also indicates:

> once new data has been written to the first (invisible framer buffer) portion 43 of the array 42, the data therein may be transferred to the second (visible frame buffer) portion 44 from which information may be scanned to the display. (col. 11, lines 22–26.) (Emphasis added.)

In other words, although new data within the invisible frame buffer may be transferred to the visible trunk buffer, data is never transferred from the invisible frame buffer to the display, as required by Claim 1.

Applicant submits that the designation of the invisible frame buffer portion of the array 42, which is never scanned to the display, prohibits the Examiner from establishing a teaching or suggestion within Priem1 to a controller to copy identified data updated within the first frame buffer to the second frame buffer and a display monitor when the identified data is needed to refresh the display monitor, as required by Claim 1.

To wit, the case law is quite clear in requiring that anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention. *Id.*

Therefore, for at least the reasons described above, Applicant respectfully submits that the Examiner has failed to establish a *prima facie* rejection of Claim 1 over Priem1. Accordingly, for at least the reasons described above, Claim 1 is patentable over Priem1 as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claim 1.

Regarding Claim 2, Claim 2 depends from Claim 1 and therefore include the patentable claim features of Claim 1. Accordingly, for at least the reasons described above, Claim 2 are patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claim 2.

Regarding Claim 26, Applicant submits that independent Claim 26 includes the following feature, which is neither taught nor suggested by either Priem1 or the references of record:

> a controller to coordinate refresh of the display monitor using data stored in the second frame buffer and data updated within the first frame buffer. (Emphasis added.)

In order to anticipate Claim 26, the Examiner must illustrate a teaching or suggestion within Priem1 to transfer of data from the invisible (first) frame buffer to the display. However, Priem1 strictly prohibits transfer of data from the first (invisible) frame buffer to the display. (*See* col. 11, lines 6–9.) (Emphasis added.)

Therefore, for at least the reasons described above, Applicant respectfully submits that the Examiner has failed to establish a *prima facie* rejection of Claim 26 over Priem1. Applicant submits that for at least the reasons described above, Claim 26 is patentable over Priem1 as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claim 26.

II. Claims Rejected Under 35 U.S.C. §103

The Patent Office rejects Claims 7-9 and 20 under 35 U.S.C. §103(a) as being unpatentable over Priem1 as applied to Claim 1 and further in view of U.S. Patent No. 5,790,138 to Hsu ("Hsu"). Applicant respectfully traverses this rejection.

Regarding Claims 7 and 8, Claims 7 and 8 are dependent from Claim 1 and therefore include the patentable claim features of Claim 1, as described above. Applicant submits that the teaching of Hsu does not rectify the deficiencies attributed to Priem1's failure to teach or suggest the controller for copying updated data from the first frame buffer to both the second frame buffer and the display memory. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 7 and 8.

Regarding Claim 9, the Examiner proposes to modify Priem1 in view of Hsu, which the Examiner believes describes a first frame buffer as part of a unified memory architecture. However, after careful review of Priem1, Applicant respectfully submits that Priem1 teaches away from providing a first memory buffer as part of a unified memory architecture.

This proposition is based on the fact that Priem1 teaches a single frame buffer, which may be configured as a pair of frame buffers. However, as described within Priem1, frame buffer 42 is nothing more than a single array of contiguous memory 42, which may be configured in various buffer arrangements in response to the software being run. As a result, modification of Priem1 to provide a first frame buffer within a unified memory architecture would require either the inclusion of an additional frame buffer or the subdivision of the frame buffer 42, as depicted in Priem1.

According to the Examiner, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Priem1 with the feature frame buffer as part of the

unified memory architecture because it provides for a lower system cost. However, the Examiner, as required by MPEP §2142, cannot show a suggestion or motivation to combine reference teachings unless there is a reasonable expectation of success in modifying the reference teachings.

The Examiner has failed to address how an additional frame buffer, incorporated into a unified memory architecture, would function in conjunction with the frame buffer 42, as described with reference to FIG. 3 of Priem1. Furthermore, the Examiner has failed to address how the frame buffer 42 of Priem1 could be subdivided such that a portion of the frame buffer is designated within the unified memory architecture.

Consequently, Applicant respectfully submits that the Examiner cannot establish a *prima facie* rejection of Claim 9 since there is no teachings or suggestions to modify Priem1 in view of Hsu in violation of MPEP §2142. Accordingly, for at least the reasons described above, Applicant respectfully submits that Claim 9 is patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 9.

Furthermore, Claim 9 includes a controller feature as described above with reference to Claim 1. As indicated, this controller feature enables an analogous simultaneous buffer refresh from both the first and second frame buffer memories in violation of the stated prohibition of Priem1 of scanning from the invisible frame buffer to the display.

Accordingly, for at least the reasons described above, Applicant respectfully submits that the Examiner cannot establish a §103(a) rejection of Claim 9 since the cited references by the Examiner do not teach each and every element of Claim 9 and the Examiner fails to establish a reasonable expectation of success in modifying the reference teachings. Consequently, for at least the reasons described above, Claim 9, as amended, is patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 9.

The Patent Office rejects Claims 3, 11 and 27 under 35 U.S.C. §103(a) as being unpatentable over Priem1 as applied to Claim 1 and further in view of U.S. Patent No. 5,724,608 to Tohara ("Tohara") and further in view of U.S. Patent No. 5,543,824 to Priem et al. ("Priem2"). Applicant respectfully traverses this rejection.

Regarding Claim 3, Claim 3 depends from independent Claim 1 and therefore includes the patentable claim features as described above with reference to Claim 1. Applicant submits that the teachings of both Tohara as well as Priem2 do not rectify the deficiencies attributed to Priem1's failure to teach or suggest the controller for copying updated data from the first frame buffer to both the second frame buffer and the display memory. Therefore, for at least the reasons described above, Claim 3 is patentable over the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 3.

Regarding Claim 11, Applicant submits that Claim 11 is dependent from Claim 9 and therefore includes the patentable claim features of Claim 9 including a controller as described above with reference to Claim 1. As indicated above, the Examiner's citing of Tohara as well as Priem2 do not rectify the deficiencies attributed to Priem1 in order to render Claim 11 obvious over Priem1 in view of Tohara and further in view of Priem2. Consequently, Applicant submits that the Examiner fails to establish a *prima facie* rejection of Claim 11 under 35 U.S.C. §103(a). Therefore, Applicant respectfully requests the Examiner reconsider and withdraw the §103(a) rejection of Claim 11.

Regarding Claim 27, Applicant submits that Claim 27 is dependent from Claim 26 and therefore includes the patentable claim features of Claim 26 including a controller as described above with reference to Claim 1. As indicated above, the Examiner's citing of Tohara as well as Priem2 do not rectify the deficiencies attributed to Priem1 in order to render Claim 27 obvious over Priem1 in view of Tohara and further in view of Priem2. Consequently, Applicant submits that the Examiner fails to establish a *prima facie* rejection of Claim 27 under 35 U.S.C. §103(a). Therefore, Applicant respectfully requests the Examiner reconsider and withdraw the §103(a) rejection of Claim 27.

The Patent Office rejects Claims 4-6, 12-15, 17-19, 21, 23-25 and 28-30 under 35 U.S.C. §103(a) as being unpatentable over Priem1 as applied to Claim 1 and further in view of Tohara and further in view of Priem2 as applied to Claim 3 and further in view of U.S. Patent No. 5,757,364 to Ozawa et al. ("Ozawa"). Applicant respectfully traverses this rejection.

Regarding Claims 4-6, Claims 4-6 depend from, and therefore include, the patentable claim features of Claim 1 as described above. Furthermore, the Examiner's citing of Tohara, Priem2 reference, as well as Ozawa, fails to rectify the deficiencies attributed to Priem1 for its failure to describe a controller which enables copying of updated data from the first frame buffer to both the display monitor and second frame buffer when required to refresh the display monitor.

Accordingly, for at least the reasons described above, Applicant respectfully submits that Claims 4-6 are patentable over the references of record. Consequently, the Examiner cannot establish a *prima facie* rejection of Claims 4-6 over Priem1 in view of Tohara and further in view of Priem2, as all as Ozawa. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 4-6.

Regarding Claims 12-14, Claims 12-14 include features of the detectors and decoders which enable the controller of Claim 9 to concurrently refresh a display monitor using data contained within a secondary frame buffer, as well as updated data contained within a primary frame buffer. Accordingly, Applicant submits that the specific prohibition against simultaneous copying from frame buffers of Priem1 prohibits the Examiner from establishing a *prima facie* rejection of

Claims 12-14. Consequently, Applicant respectfully requests the Examiner reconsider and withdraw the §103(a) rejection of Claims 12–14.

Regarding Claim 15, Claim 15 includes the following feature, which is neither taught nor suggested by the references of record:

> coordinating refreshing of the display monitor and copying identified data from the first frame buffer memory to a second frame buffer memory and a display monitor when the data is needed to refresh the display monitor. (Emphasis added.)

As indicated above, this feature is specifically taught away from in Priem1 by Priem1's prohibition against copying from the invisible frame buffer to the display. Accordingly, based on the specific prohibit against data transfer from the invisible frame buffer to the display, Applicant submits that the Examiner cannot establish a *prima facie* rejection of independent Claim 15 over either Priem1 in view of Tohara and further in view of Priem2 as well as Ozawa. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 15.

Regarding Claims 17-19, Claims 17-19 depend from Claim 15 and therefore include the patentable claim features of Claim 15 as described above. Accordingly, for at least the reasons described above, Claims 17-19 are patentable over the references of record. Consequently, Applicant respectfully requests the Examiner reconsider and withdraw the §103(a) rejection of Claims 17-19.

Regarding Claim 21, Claim 21 includes analogous features to Claim 15 as described above in the form of a computer program product. Accordingly, for at least the reasons described above with reference to Claim 15, Applicant respectfully submits that the Examiner cannot establish a *prima facie* rejection of Clam 21 over the references of record. Consequently, Applicant respectfully requests the Examiner reconsider and withdraw the §103(a) rejection of Claim 21.

Regarding Claims 23-25, Claims 23-25 depend from Claim 21 and therefore include the patentable claim features of Claim 21 as described above. Consequently, Applicant respectfully submits that Claims 23-25 are patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 23–25.

Regarding Claims 28-30, Claims 28-30 depend from, and therefore include, the patentable claim features of Claim 26 as described above. Furthermore, the Examiner's citing of Tohara, Priem2 reference, as well as Ozawa, fails to rectify the deficiencies attributed to Priem1 for its failure to describe a controller which enables copying of updated data from the first frame buffer to both the display monitor and second frame buffer when required to refresh the display monitor.

Accordingly, for at least the reasons described above, Applicant respectfully submits that Claims 28-30 are patentable over the references of record. Consequently, the Examiner cannot

establish a *prima facie* rejection of Claims 28-30 over Priem1 in view of Tohara and further in view of Priem2, as all as Ozawa. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 28-30.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Dated: September 19, 2003

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. 1450, Alexandria, VA 22313-1450 on September 19 2003.

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Marilyn Bass September 19, 2003